*Data Sheet*
*May 2012*

# MAX24188 EV KIT
# Evaluates: MAX24188

## General Description

The MAX24188 EV Kit is an easy-to-use evaluation kit for the MAX24188 Low-Cost IEEE1588 Time Clock. An on-board high-stability TC-OCXO oscillator is provided to allow evaluation of 1588 performance with a variety of network PDV and impairment scenarios. Also, the board can accept an external oscillator input for testing alternate oscillators. The board provides SMB connectors for three device GPIO signals. Through these connectors clock and 1PPS signals can be input or output to lock the MAX24188 time clock to a master time clock or to lock other 1588 components to the MAX24188.

Typically the board is controlled by EV kit software running on a Windows PC through the USB interface. The board also has SPI and JTAG headers through which the MAX24188 can be controlled by a processor on another board as needed.

## Features

- GPIO SMB Connectors to Input or Output Clock Signals and 1PPS Signals
- Onboard TC-OCXO Provides Stable Reference for High-Quality Timing over IEEE1588
- Connectors and Component Sites for Alternate Oscillators as Needed
- Included Universal 5V Power Supply
- Jumpers to Configure Reset State of MAX24188, GPIO Termination, and More
- LEDs for Power Supplies Valid and Port Status
- Soldered MAX24188 for Best Signal Integrity
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs
- Windows®-Based Evaluation Software Provides Easy Configuration and Monitoring of the MAX241888 Device
- Evaluation Software Calls MAX24188 HAL Software and Structure is Similar to HAL Software

## Demo Kit Contents

- MAX24188 Board
- Power Supply
- USB Cable

*Ordering Information appears at end of data sheet.*

## Minimum System Requirements

- PC Running Windows XP or later
- Available USB Port

# Contents

## List of Figures



## List of Tables

## 1. Board Floorplan

When the board is oriented as shown in Figure 1, The 5V power supply and USB cable included with the kit are connected to jacks J1 and J2 at the top of the board. The board ships with a TCXO mounted in the Y3 oscillator position and a 25MHz XO in the Y1 position. See section 6 for detailed descriptions of the board's jumpers, connectors and LEDs. The same PCB is also used for the MAX24288 EV kit, and many components needed for the MAX24288 EV kit are not populated for the MAX24188 EV kit including U5, U7, J29 and J31.

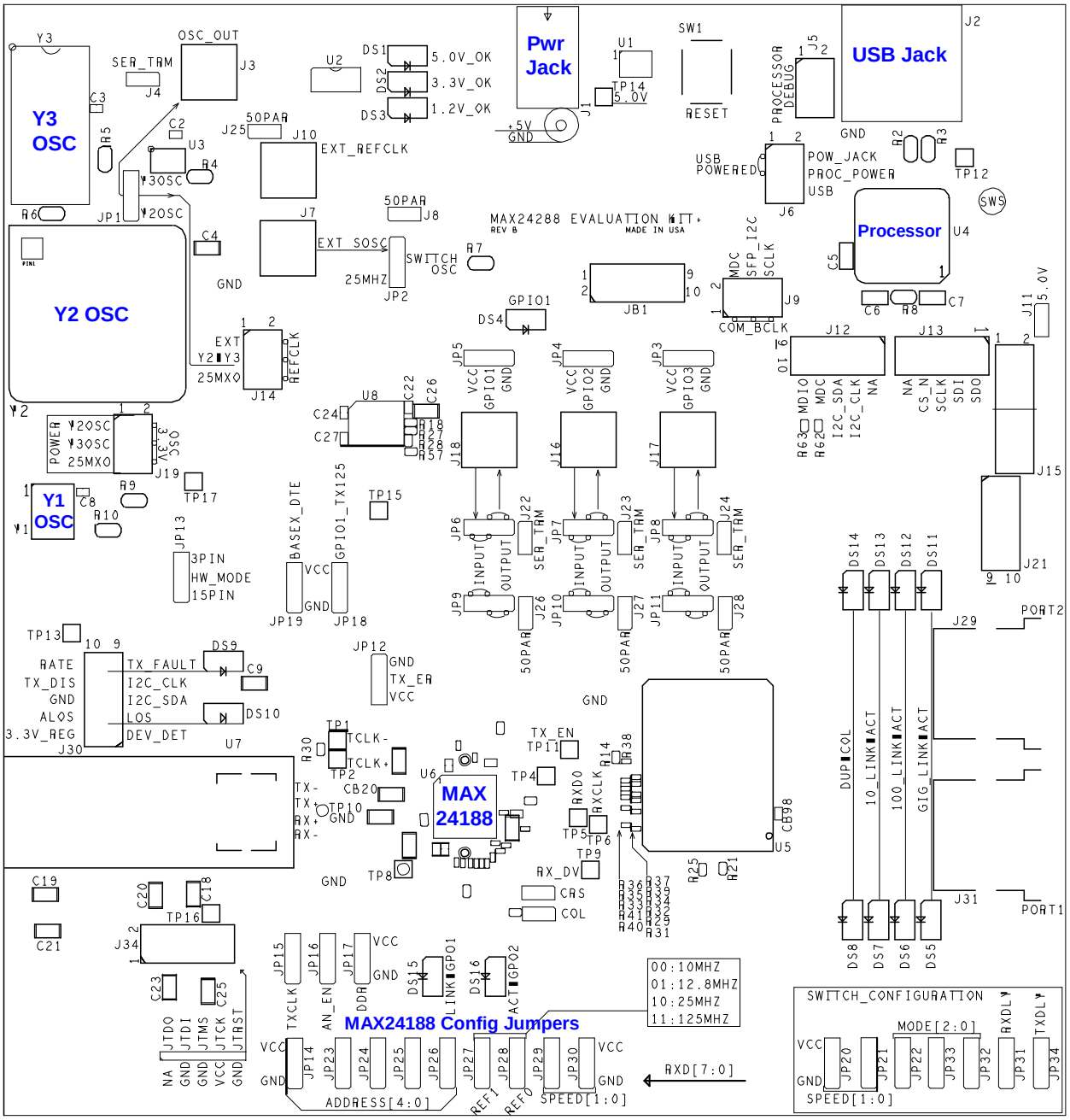



**Figure 1. MAX24188 EV Kit Board Floorplan**

# 2. Connections to the Board

## 2.1 Power-Supply Connection

The board is powered through connector J1 using the provided AC wall-plug 5V power supply. LED DS1 illuminates to indicate that the board is powered.

## 2.2 USB Connection

The MAX24188 EV kit software application communicates with the EV kit board through USB connector J2.

## 2.3 Example Setup

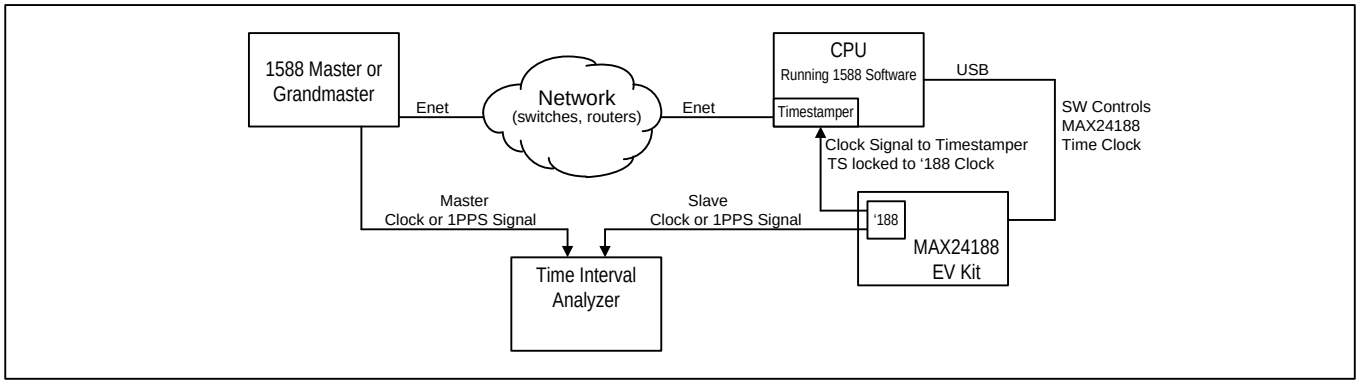



**Figure 2. Example Setup**

# 3. Installing the Software

**Important Note:** *Do not connect the board to the PC until after installing the software*. The device driver for the USB microcontroller will not be installed correctly.

Follow these steps to install the MAX24188 EV Kit software:

1. To install the software, run max24188evk.exe. The latest version of the EV Kit software can be downloaded from the Microsemi website or requested from Microsemi timing products technical support.
2. In the window that indicates the publisher could not be verified, click **Run**.
3. Follow the prompts in the MAX24188 Eval Kit setup wizard, For a default installation, click **Next** three times.
4. Connect the power cord to the J1 connector on the EV Kit board.
5. Connect a USB cable from a USB jack on the PC to the J2 connector on the EV Kit board.
6. In the notification area, Windows will indicate “Installing device driver” and then indicate “Freescale CDC Device (COM6) Device driver software installed successfully.”

   The text “COM6” indicates the virtual COM port number assigned to the board. This number varies from system to system. Write down the assigned number to use when running the EV Kit software.

   If Windows does not show the messages above then verify that the board is powered and is connected to the PC. If the board was already connected to the PC before installing the software then see follow the troubleshooting steps in section 3.1.

## 3.1 Troubleshooting Software Installation

If the board was connected to the PC before installing the software or if the EV kit software does not list the board’s COM port number as an option, then follow these steps:

1. In Windows, go to the Device Manager. In recent versions of Windows this is done by going to **Control Panel** and double-clicking **System.** Then in the upper-left corner click **Device Manager**.

2. In the Device Manager window, under **Other devices**, right-click on **Unknown device** and select **Uninstall**. In the **Confirm Device Uninstall** pop-up click **OK**.
3. In **Control Panel** double-click **Programs and Features**.
4. Right-click on **MAX24188 Eval Kit** and select **Uninstall**.
5. Disconnect power and USB cables from the EV Kit board.
6. Follow the steps in section 3.

## 4. Running the Software

To run the software, double-click on the **MAX24188 Eval Kit** shortcut on the desktop, or in the Windows Start menu, select **All Programs → Microsemi → MAX24188 Eval Kit**.

At the prompt enter the COM port number assigned to the board in step 6 in section 3.

The software then displays its main menu, as shown in Figure 2.

To start communication with the MAX24188 on the EV kit board, type **1** then **Enter** to create the MAX24188 HAL. If the software and the USB device driver have been installed correctly then regular screen updates begin, the **TE SEC** field increments once per second, and **TE NS** fields displays ever-changing values.

If the software exits unexpectedly then run the software again and specify a different COM port number. If none of the listed COM port numbers is correct then follow the troubleshooting steps in section 3.1.

## 5. Software User Interface

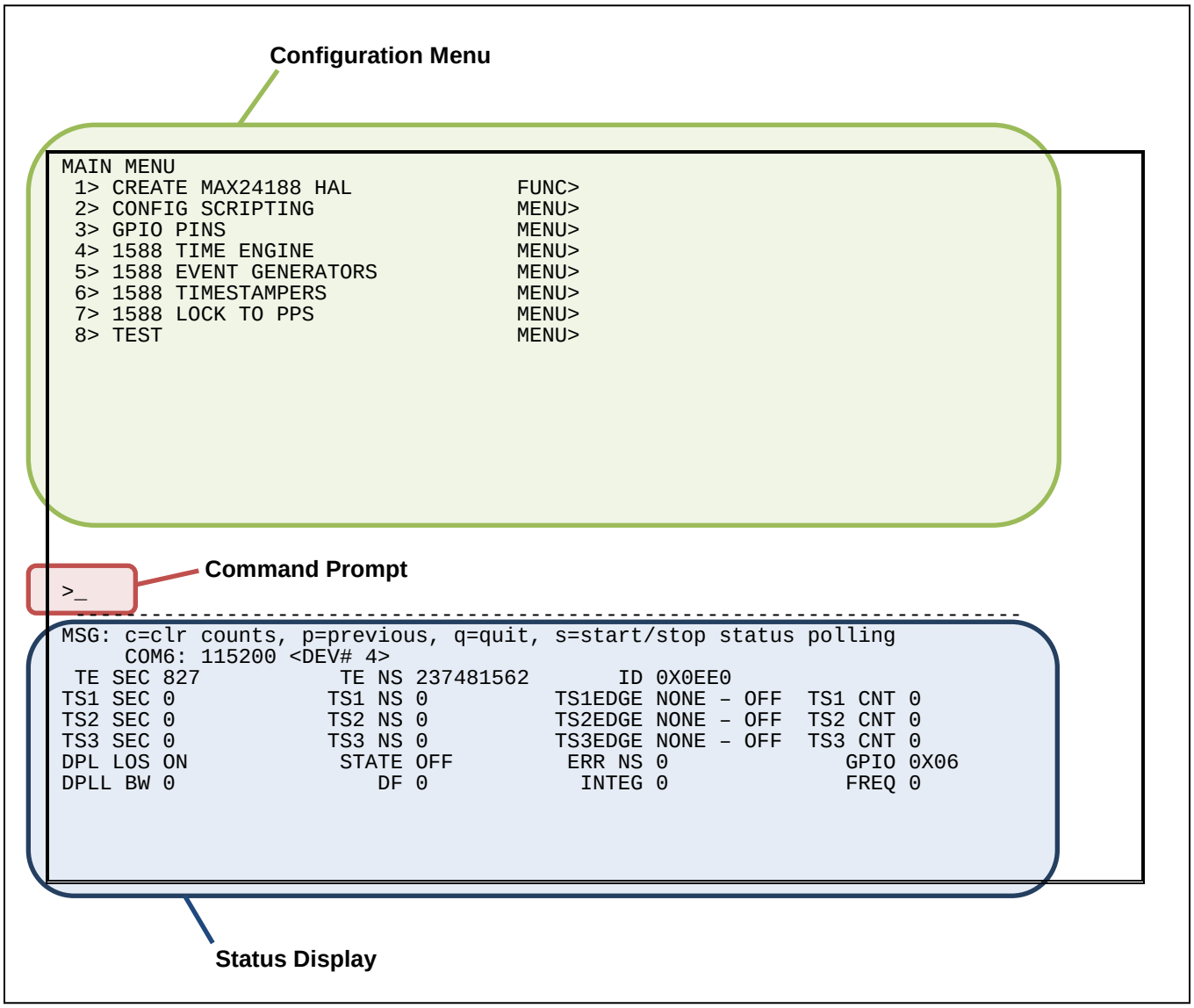



**Figure 3. User Interface Main Screen**

### 5.1 Status Display

The status display area (see the bottom of Figure 2) shows the latest data polled from the device. To start software polling and updating of these fields, select **CREATE MAX24188 HAL** in the main menu. To start or stop polling, use the **s** command at the command prompt. Table 1 lists and describes the status display fields.

**Table 1. Status Display Fields**

| Row | Field | Description |
|---|---|---|
| 1 | TE SEC | Time engine seconds field |
| 1 | TE NS | Time engine nanosecond field |
| 1 | ID | Value read from the MAX24188 ID register |
| 2 | TS1 SEC | Timestamper 1, timestamp seconds field |
| 2 | TS1 NS | Timestamper 1, timestamp nanoseconds field |
| 2 | TS1EDGE | Timestamper 1, timestamp edge type, 0=falling, 1=rising |
| 2 | TS1 CNT | Count of timestamps done by timestamper 1 since HAL started or last **c** command. |
| 3 | TS2 SEC | Timestamper 2, timestamp seconds field |

| Row | Field | Description |
|---|---|---|
| 3 | TS2 NS | Timestamper 2, timestamp nanoseconds field |
| 3 | TS2EDGE | Timestamper 2, timestamp edge type, 0=falling, 1=rising |
| 3 | TS2 CNT | Timestamper 2, count of timestamps done since HAL started or last **c** command |
| 4 | TS3 SEC | Timestamper 3, timestamp seconds field |
| 4 | TS3 NS | Timestamper 3, timestamp nanoseconds field |
| 4 | TS3EDGE | Timestamper 3, timestamp edge type, 0=falling, 1=rising |
| 4 | TS3 CNT | Timestamper 3, count of timestamps done since HAL started or last **c** command. |
| 5 | DPL LOS | Hardware/Software DPLL loss of signal |
| 5 | STATE | Hardware/Software DPLL state |
| 5 | ERR NS | Hardware/Software DPLL time error in nanoseconds |
| 5 | GPIO | MAX24188 GPIO status register (GPIOSR) bits 6:0 |
| 6 | DPLL BW | Hardware/Software DPLL bandwidth |
| 6 | DF | Hardware/Software DPLL damping factor |
| 6 | INTEG | Hardware/Software DPLL integral path control |
| 6 | FREQ | Hardware/Software DPLL frequency control |

## 5.2 Configuration Menu and Command Prompt

### 5.2.1 Navigating Menus and Changing Settings

Figure 3 shows the main screen of the MAX24188 software. In the upper half of the screen the command menu has two columns. The left-hand column shows numbered command/menu options. The right-hand column indicates what happens when an option is chosen. **FUNC>** indicates that a function is executed, **LIST>** indicates a list of choices will be presented, and **MENU>** indicates that the user will be taken to a submenu. Data types such as **UINT32>** or **STR>** indicate that a value with the specified data type can be entered. **UINT32>**, for example, means a 32-bit unsigned integer. **STR>** means text string.

To change the device configuration, the user types a number at the command prompt followed by the **Enter** key. If the option selected has a data type in the right-hand column, such as **UINT32>** then the cursor moves to the right of the data type. The user then enters the desired value followed by the **Enter** key. The cursor then moves back to the command prompt area.

If the option selected has **LIST>** in the right-hand column, then the cursor moves to the right of the **LIST>** text and a list of options is shown in an additional column on the right. The user then enters the option number from the list followed by the **Enter** key. The value next to **LIST>** then changes to the option selected, and the cursor moves back to the command prompt area.

### 5.2.2 Configuring the Device

All menus of the software are designed to have a two-step configuration process:

1. Configure the relevant values using data-type or **LIST>** menu options.
2. Configure the HAL or the device using a **FUNC>** menu option.

For example, in the **GPIO PINS** menu, some or all of the parameters in the menu are configured and then **CONFIG GPIO** is selected to write MAX24188 device registers.

### 5.2.3 Other Commands

In addition to menu item numbers, the following commands are also valid at the command prompt:

**c** – clear counts in status area
**p** – return to previous menu (when in a submenu)
**q** – quit the program
**s** – stop/start status polling

## 5.3 Configuration Menu Detailed Descriptions

**Table 2. MAIN Menu**

| Name | Description |
|---|---|
| CREATE MAX24188 HAL | This function creates the MAX24188 HAL and starts polling device status. The three MAX24188* fields below must be set before this function is executed. |
| CONFIG SCRIPTING | Opens the CONFIG SCRIPTING menu. See Table 13. |
| GPIO PINS | Opens the GPIO PINS menu. See Table 14. |
| 1588 TIME ENGINE | Opens the 1588 TIME ENGINE menu. See Table 16. |
| 1588 EVENT GENERATORS | Opens the 1588 EVENT GENERATORS menu. See Table 17. |
| 1588 TIMESTAMPERS | Opens the 1588 TIMESTAMPERS menu. See Table 19. |
| 1588 LOCK TO PPS | Opens the 1588 LOCK TO PPS menu. See Table 27. |
| TEST | Opens the TEST menu. See Table 28. |

**Table 3. CONFIG SCRIPTING Menu**

| Name | Description |
|---|---|
| READ CONFIGURATION | Function reads configuration information from the file specified by the READ CONFIG FILE NAME parameter below. |
| WRITE CONFIGURATION | Function writes configuration information to the file specified by the WRITE CONFIG FILE NAME parameter below. |
| READ CONFIG FILE NAME | The file name for the READ CONFIGURATION function above. The file extension is .cfg. |
| WRITE CONFIG FILE NAME | The file name for the WRITE CONFIGURATION function above. The file extension is .cfg. |

**Table 4. GPIO PINS Menu**

| Name | Description |
|---|---|
| CONFIG GPIO | Function writes GPIO configuration from the fields below to MAX24188 register GPIOCR1 or GPIOCR2 for the pin(s) specified by GPIO CONFIG SELECT below. |
| GPIO CONFIG SELECT | Specifies one or all of {GPO1, GPO2, GPIO1-7} to be configured by the CONFIG GPIO function above. |
| GPOx MODE, GPIOx MODE (9 fields total) | Specify high-impedance, low, high, and several other options. Other options are pin-dependent and include:<br>INT = interrupt output<br>EXT CLK = Output the PTP_CLKO signal from the time engine<br>REFCLK PLL 125 MHZ = Output 125MHz from the reference clock PLL<br>RX 125/25 MHZ = Output clock from receive clock recovery PLL; the frequency is specified by GPIO RX PLL CLK MODE in the DATA PATH menu.<br>RX 125/25 MHZ SQUELCH = same as RX 125/25 MHZ above and the output clock signal is squelched when certain receiver conditions occur such as LOS or ALOS<br>LOS or ALOS = Output real-time link status, 1= link up<br>CRS = Output carrier sense status<br>PEG1 = Output signal generated by Programmable Event Generator 1<br>PEG2 = Output signal generated by Programmable Event Generator 2<br>See Table 6-4 through Table 6-6 in the MAX24188 data sheet.<br>Note that GPIO4 through GPIO7 are the TXD4 through TXD7 pins, which are not available when the parallel MII interface is configured as GMII. |

**Table 5. 1588 TIME ENGINE Menu**

| Name | Description |
|---|---|
| SET TIME | Function writes time from TIME SEC and TIME NS below to the MAX24188 time engine. |
| TIME SEC | Specifies the seconds portion of the time for the SET TIME function above.<br>*Affects the MAX24188 TIME register field.* |
| TIME NS | Specifies the nanoseconds portion of the time for the SET TIME function above.<br>*Affects the MAX24188 TIME register field.* |
| SET FREQ OFFSET | Function adjusts the MAX24188 PERIOD register from its nominal value of 8.0ns by the amount specified in the FREQ OFFSET field below. |
| FREQ OFFSET +/- PPT | Specifies a time engine frequency offset in parts per trillion (PPT).<br>*Affects the MAX24188 PERIOD register field.* |
| DO TIME BUILD OUT | Function adjusts MAX24188 time engine time smoothly. Time is advanced by the amount specified by TBO ADJUSTMENT (below) over a duration specified by TBO DURATION (below). For example, if TBO ADJUSTMENT is 100ns and TBO DURATION is 1s then DO TIME BUILD OUT advances time in the MAX24188 time |

| Name | Description |
|---|---|
| | engine by an extra 100ns, but it does this extra advance at a rate of 100ns/1s=0.1ppm.<br>DO TIME BUILD OUT makes one-time or repeated used of the precise time adjustment feature described in section 6.13.1.3 of the MAX24188 data sheet.<br>*Affects register fields PER_ADJ and ADJ_CNT.* |
| TBO DURATION +/- NS | Specifies the total time duration during which the time is adjusted by the DO TIME BUILD OUT function above. |
| TBO ADJUSTMENT +/- NS | Specifies the total time adjustment desired for the DO TIME BUILD OUT function above. |
| CONFIG EXT CLK & PTP_CLKO | Function configures the MAX24188 external clock and PTP_CLKO output clock features using the settings of the EXT CLK SOURCE through PTP_CLKO INVERT fields below. See MAX24188 data sheet section 6.13.1.4 for more information about the external clock syntonization feature. See MAX24188 data sheet section 6.13.2 for more information about the PTP_CLKO output clock. |
| EXT CLK SOURCE | Specifies the input signal pin for the MAX24188 external clock syntonization feature.<br>*Affects register field PTPCR3.EXT_SRC.* |
| EXT CLK ENABLE | Enable/disable control for the MAX24188 external clock syntonization feature.<br>*Affects register field PTPCR3.EXT_CLK_ENA.* |
| EXT CLK DIVIDE | Specifies the external clock divider value.<br>*Affects register field PTPCR3.EXT_DIV.* |
| EXT CLK LIMIT | Specifies the maximum number of nanoseconds to adjust the time engine accumulator period from the nominal value set by the MAX24188 PERIOD register.<br>*Affects register field PTPCR3.EXT_LIM.* |
| EXT CLK PER NS (16-255) | Specifies the period of the external clock after being divided by the EXT CLK DIVIDE value.<br>*Affects register field PTPCR3.EXT_PER.* |
| PTP_CLKO DIVIDE (0=NO DIV) | Specifies the divide value for the PTP_CLKO signal. PTP_CLKO frequency is 125MHz divided by this value.<br>*Affects register field PTPCR2.CLKO_DIV.* |
| PTP_CLKO INVERT | Invert/non-invert control.<br>*Affects register field PTPCR2.CLKO_INV.* |

**Table 6. 1588 EVENT GENERATORS Menu**

| Name | Description |
|---|---|
| CONFIG PEG | Function configures the MAX24188 programmable event generator(s) (PEGs) using settings from the fields below and the PEG1 COMMMANDS and PEG2 COMMANDS submenus. |
| PEG CONFIG SELECT | Specifies one or both of the PEGs to be configured by the CONFIG PEG function above. |
| PEG1 MODE | Allows the user to specify that PEG1 generate one of several common clock frequencies from 0.5Hz through 31.25MHz. If the CUSTOM option is selected then the user can specify a custom PEG command script in the PEG1 COMMANDS submenu. |
| PEG1 OFFSET NS | When PEG1 MODE≠CUSTOM then this field specifies an offset from the one-second boundary for the first edge generated by the PEG. If PEG1 OFFSET=0 then PEG1 is configured to generate the first output signal edge when the time engine's nanosecond field equals 0. If, for example, PEG1 OFFSET=-10 then PEG1 is configured to generate the first output signal edge when the time engine's nanoseconds field equals 999,999,990 (i.e. 10ns before the nanoseconds field rolls over to 0). |
| PEG2 MODE | Same as PEG1 MODE above but for PEG2. |
| PEG2 OFFSET NS | Same as PEG1 OFFSET above but for PEG2. |
| PEG1 COMMANDS | Opens the PEG1 COMMANDS Menu where a custom PEG1 command script can be entered. See Table 18. |
| PEG2 COMMANDS | Same as PEG1 COMMANDS above but for PEG2. |

**Table 7. PEG1/PEG2 COMMANDS Submenu**

| Name | Description |
|---|---|
| CMD RESOLUTION | Specifies 1ns or 1/256ns resolution for the 16-bit and 32-bit relative time commands written to the PEG command FIFO.<br>*Affects register field PEGCR.P1RES for PEG1 and PEGCR.P2RES for PEG2.* |
| CMD WORD LENGTH | Specifies the number of words of CMD WOR 0 through CMD WORD 15 below that the software should write to the PEG command FIFO. CMD WORD LENGTH=1 indicates that only CMD WORD 0 should be written. CMD WORD LENGTH=4 indicates that CMD WORD 0 through CMD WORD 3 should be written. |
| CMD WORD 0 –<br>CMD WORD 15 | Specifies up to 16 entries to be written to the PEG command FIFO. The CMD WORD LENGTH field above specifies the number of entries that are written to the PEG command FIFO. |

**Table 8. 1588 TIMESTAMPERS Menu**

| Name | Description |
|---|---|
| CONFIG TS | Function configures the MAX24188 timestampers using settings from the fields below and the PACKET TS FIFO ENABLES submenu. |
| TS CONFIG SELECT | Specifies one or all of the timestampers to be configured by the CONFIG TS function above. |
| TS1 SOURCE | Specifies the source of the signal to be timestamped by timestamper 1.<br>*Affects register field TSCR.TS1SRC_SEL.* |
| TS1 EDGE | Specifies whether positive edges, negative edges or both should be timestamped by timestamper 1.<br>*Affects register field TSCR.TS1EDGE.* |
| TS1 OFFSET NS | Specifies an offset in nanoseconds that software adds to each timestamp generated by the MAX24188. This field allows software to correct for cable delays, signal skews, etc. |
| TS1 DIVIDER 1 | Specifies the timestamper 1 divider 1 setting. One or both of the TS1 dividers can be used to divide down the frequency of the input signal that goes to timestamper 1 in order to reduce the number of edges that must be timestamped. The input signal frequency is divided by value entered + 1.<br>*Affects register field TS1_DIV1.* |
| TS1 DIVIDER 2 | Specifies the timestamper 1 divider 2 setting.<br>*Affects register field TSCR.TS2SRC_SEL.* |
| TS2 SOURCE | Specifies the source of the signal to be timestamped by timestamper 2.<br>*Affects register field TSCR.TS2SRC_SEL.* |
| TS2 EDGE | Specifies whether positive edges, negative edges or both should be timestamped by timestamper 2.<br>*Affects register field TSCR.TS2EDGE.* |
| TS2 OFFSET NS | Same as TS1 OFFSET NS above but for timestamper 2. |

| Name | Description |
|---|---|
| TS3 SOURCE | Specifies the source of the signal to be timestamped by timestamper 3.<br>*Affects register field TSCR.TS3SRC_SEL.* |
| TS3 EDGE | Specifies whether positive edges, negative edges or both should be timestamped by timestamper 3.<br>*Affects register field TSCR.TS3EDGE.* |
| TS3 OFFSET NS | Same as TS1 OFFSET NS above but for timestamper 3. |

**Table 9. LOCK TO PPS Menu**

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>CONFIG LOCK TO PPS</td><td>Function configures the evaluation software using settings from the fields below to work with the MAX24188 hardware to form a hardware/software PLL that locks to an input 1PPS signal. In this PLL, timestamper 1 (TS1) in the MAX24188 timestamps edges of a 1PPS input signal. The edges of this signal are assumed to occur at the exact one-second boundary. Therefore ideally the timestamp nanoseconds field should be 0. The difference between the nanosecond field and zero is the error information used to control the PLL.<br>Note 1: TS1 must be configured to timestamp an input 1PPS signal in the 1588 TIMESTAMPERS Menu (Table 19) before executing the CONFIG LOCK TO PPS function.<br>Note 2: The evaluation software controls the time and/or frequency of the MAX24188 time engine when PLL MODE below is not OFF. Therefore previous settings of time engine values may be overwritten by the evaluation software when the LOCK TO PPS PLL is enabled.</td></tr>
<tr><td>PLL MODE</td><td>Specifies operating mode of the hardware/software PLL.
<table>
<tr><th>Mode</th><th>Description</th></tr>
<tr><td>OFF</td><td>Disable the PLL</td></tr>
<tr><td>FREERUN</td><td>Ignore error information from TS1 and clock the time engine at the frequency specified by the FREE RUN FREQ PPM field below.</td></tr>
<tr><td>FREQ MEASURE</td><td rowspan="6">For debug only. These values force the hardware/software PLL into a particular operating state.</td></tr>
<tr><td>FREQ ADJUST</td></tr>
<tr><td>TIME ADJUST</td></tr>
<tr><td>TIME MEASURE</td></tr>
<tr><td>TIME BUILD OUT</td></tr>
<tr><td>LOCK</td></tr>
<tr><td>HOLDOVER</td><td>Ignore error information from TS1 and clock the time engine at a holdover frequency averaged by the evaluation software while the PLL was locked to an input signal.</td></tr>
<tr><td>AUTO FREQ LOCK</td><td>Fully automatic PLL operation with frequency-only locking. When the PLL is locked its output frequency tracks the frequency of the input signal, but time is not adjusted. Therefore the MAX24188 time engine will have a fixed time offset vs. the source of the input signal.</td></tr>
<tr><td>AUTO TIME LOCK</td><td>Fully automatic PLL operation with time-and-frequency locking. When the PLL is locked the time and frequency of the MAX24188 time engine track the input signal.</td></tr>
</table></td></tr>
<tr><td>EVENTS PER SECOND</td><td>Specifies the number of edges per second in the input signal timestamped by TS1. For a 1PPS signal this field should be set to 1.</td></tr>
<tr><td>FREERUN FREQ PPM</td><td>Specifies a frequency offset vs. the frequency accuracy of the REFCLK oscillator for when PLL MODE above is set to FREERUN.</td></tr>
<tr><td>FREQ RATE OF CHANGE PPM/SEC</td><td>Specifies the maximum frequency rate of change that the evaluation software can use when locking to an input signal.</td></tr>
<tr><td>PLL BANDWIDTH, HZ</td><td>Specifies the bandwidth of the hardware/software PLL in Hz.</td></tr>
<tr><td>PLL DAMPING FACTOR</td><td>Specifies the damping factor of the hardware/software PLL. A typical value is 5. Larger numbers provide more damping, i.e. less peaking at the PLL corner frequency.</td></tr>
</table>

**Table 10. TEST Menu**

| Name | Description |
|---|---|
| READ REGISTER | Function reads the register specified by the REGISTER ADDRESS fields below and displays the value in the REGISTER DATA fields below. |
| WRITE REGISTER | Functions writes the data value specified in the register data fields below into the register address specified by the REGISTER ADDRESS fields below. |
| REGISTER ACCESS MODE | Specifies the register access mode.<br>MAX24188 USER MODE: The registers in Table 7-1 of the MAX24188 data sheet are at addresses 0-31 decimal, and the registers in Table 7-2 of the MAX24188 data sheet are at 32 (decimal) + SPI address.<br>SW PHY0 (MDIO#8): Accesses the registers of PHY0 on the evaluation board's switch chip.<br>SW PHY1 (MDIO#9): Accesses the registers of PHY1 on the evaluation board's switch chip.<br>SW MAC (MDIO#A): Accesses the MAC registers of the evaluation board's switch chip for the port connected to the MAX24188.<br>SFP CFG (I2C#A0): Accesses the SFP module's internal EEPROM memory.<br>SFP PHY (I2C#AC): Accesses the SFP module's PHY registers. |
| REGISTER ADDRESS HEX | Specifies the register address in hexadecimal for the READ REGISTER and WRITE REGISTER functions above. When REGISTER ADDRESS DEC below is changed, this field is changed to match. The REGISTER ACCESS MODE field above specifies the register mapping. |
| REGISTER ADDRESS DEC | Specifies the register address in decimal for the READ REGISTER and WRITE REGISTER functions above. When REGISTER ADDRESS HEX above is changed, this field is changed to match. |
| REGISTER DATA HEX | Indicates the data value in hexadecimal from the last time the READ REGISTER function was executed or the last time one of the REGISTER DATA fields was change by the user. |
| REGISTER DATA DECIMAL | Indicates the data value in decimal from the last time the READ REGISTER function was executed or the last time one of the REGISTER DATA fields was change by the user. |
| READ SFP MODULE INFO | Functions reads and displays the data from the evaluation board's SFP module. To end the data display and return to the menu, press the ENTER key. |

# 6. Jumpers, Connectors and LEDs

**Table 11. Power and Reset Components**

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| J1 | 5V jack | Connected | 4 | Power jack for 5V wall adapter (supplied) |
| DS1<br>DS2<br>DS3 | 5.0V_OK LED<br>3.3V_OK LED<br>1.2V_OK LED | On | 4 | Lit when power is within range for 5V, 3.3V, and 1.2V, respectively |
| SW1 | DUT_RST button | Unused | 5 | Manual reset for entire system |

**Table 12. MAX24188 REFCLK Jumpers and Connectors**

**Note**: MAX24188 is intolerant of REFCLK signal changes during operation. To make REFCLK signal changes, power down the board, change the jumpers as needed then apply power to the board again.

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| JP1 | Y2OSC / Y3OSC selection 3-pin header | Jumper connecting pins 2 and 3 | 7 | Drives SMB connector J3 and jumper J14 pin 1.<br>Connect the Y3OSC pin to the center pin to connect the Y3 oscillator output to J3 and J14.<br>Connect the Y2OSC pin to the center pin to connect the Y2 oscillator output to J2 and J14. |
| J3 | OSC_OUT SMB connector | Not monitored | 7 | J3 is driven by a buffer sourced by the center pin of JP1. |
| J4 | SER_TRM 2-pin header | Not monitored | 7 | Install a jumper on J4 to apply 50 ohm parallel termination to J3 |
| J10 | EXT_REFCLK SMB connector | Not monitored | 7 | External REFCLK oscillator input. Signal goes to J14 pin 1. |
| J25 | 50PAR 2-pin header | Not monitored | 7 | Jumper J25 to apply 50 ohm parallel termination to J10. |
| J14 | REFCLK 2x3pin header | Jumper connecting pins 5 and 6 | 7 | Connects 25MHz XO clock or Y2/Y3 clock or external clock to MAX24188 REFCLK pin. Frequency must match the settings of the REF[1:0] jumpers (see Table 3).<br>Connect pins 1 and 2 to select the external clock signal from SMB J10.<br>Connect pins 3 and 4 to select the Y2 or Y3 clock signal from JP1.<br>Connect pins 5 and 6 to select the Y1 clock signal. |
| J19 | OSC 3.3V POWER 2x3pin header | All jumpered | 7 | Connect/disconnect 3.3V power for oscillator components Y1, Y2 and Y3.<br>Connect pins 1 and 2 to power Y3<br>Connect pins 3 and 4 to power Y2<br>Connect pins 5 and 6 to power Y1<br>Note: the silkscreen mistakenly has Y2OSC and Y3OSC labels swapped. |

**Table 13. MAX24188 Pin Configuration Jumpers**

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| JP27<br>JP28 | REF[1:0] 3-pin headers | JP27: VCC<br>JP28: GND | 3 | MAX24188 RXD[3:2] pins. At reset the values on these pins are latched into the internal REFCLK frequency register. 00=10MHz, 01=12.8MHz, 10=25MHz, 11=125MHz. |

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP23, JP24, JP25, JP26, JP29, JP30 | Various labels 3-pin header | Not Jumpered | various | Not used in MAX24188 EV Kit |

**Table 14. MAX24188 GPIO1 Jumpers and Connectors**

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| J18 | SMB Connector | Not jumpered | 3 | I/O connector for GPIO1. |
| JP5 | GPIO1 3-pin header | Not jumpered | 3 | Can be used to bias GPIO1 high or low. |
| JP6 and JP9 | 3-pin headers | Not jumpered | 3 | To drive a signal from SMB J18 to GPIO1, jumper JP6 2-3 and JP9 2-3. To drive a signal from GPIO1 to SMB J18, jumper JP6 1-2 and JP9 1-2. |
| J22 | 2-pin header | Not jumpered | 3 | Install J22 to short the 30 ohm series termination at JP6.2. |
| J26 | 2-pin header | Not jumpered | 3 | Install J26 to apply 50 ohm parallel termination to JP9.2 |
| DS4 | LED | Off | 3 | Lit when GPIO1 is high. |

**Table 15. MAX24188 GPIO2 Jumpers and Connectors**

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| J16 | SMB Connector | Not jumpered | 3 | I/O connector for GPIO2. |
| JP4 | GPIO1 3-pin header | Not jumpered | 3 | Can be used to bias GPIO2 high or low. |
| JP7 and JP10 | 3-pin headers | Not jumpered | 3 | To drive a signal from SMB J16 to GPIO2, jumper JP7 2-3 and JP10 2-3. To drive a signal from GPIO1 to SMB J16, jumper JP7 1-2 and JP10 1-2. |
| J23 | 2-pin header | Not jumpered | 3 | Install J23 to short the 30 ohm series termination at JP7.2. |
| J27 | 2-pin header | Not jumpered | 3 | Install J27 to apply 50 ohm parallel termination to JP10.2 |

**Table 16. MAX24188 GPIO3 Jumpers and Connectors**

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| J17 | SMB Connector | Not jumpered | 3 | I/O connector for GPIO3. |
| JP3 | GPIO1 3-pin header | Not jumpered | 3 | Can be used to bias GPIO3 high or low. |
| JP8 and JP11 | 3-pin headers | Not jumpered | 3 | To drive a signal from SMB J17 to GPIO3, jumper JP8 2-3 and JP11 2-3. To drive a signal from GPIO1 to SMB J17, jumper JP8 1-2 and JP11 1-2. |
| J24 | 2-pin header | Not jumpered | 3 | Install J24 to short the 30 ohm series termination at JP8.2. |
| J28 | 2-pin header | Not jumpered | 3 | Install J28 to apply 50 ohm parallel termination to JP11.2 |

**Table 17. Processor and Debug Jumpers and Connectors**

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| J2 (USB) | USB jack | Connected | 8 | USB connector, attach to PC with supplied cable |
| J5 | PROCESSOR DEBUG 2x3pin header | Not Connected | 8 | BDM connector for use with debug pod |

| COMPONENT | LABEL AND TYPE | BASIC SETTING | SCHEMATIC PAGE | DESCRIPTION |
|---|---|---|---|---|
| J9 | COM_BCLK 2x3pin header | Not jumpered | 5 | Used to make a common communication clock. Jumper options allow to short MDC, I2C_CLK and SPI clock. |
| J12 | 2x5pin header | Jumpered 3-4, 5-6, 7-8, 9-10 | 5 | Not used in MAX24188 EV Kit. |
| J13 | 2x5pin header | Jumpered 1-2, 3-4, 5-6, 7-8 | 5 | Connection points for processor pins to MAX24188 SPI. Disconnect if connecting an external processor. |
| J15 | 2x7 header | Not used | 5 | Connection for external processor board |
| J21 | 2x5 header | Not used | 5 | SPI bus connection to external board such as Microsemi's DS31400DK. |
| J11 | 2-pin header | Not used | 5 | Place a jumper to connect 5V to J15 pin 2. |
| J34 | 2x5pin header | Jumpered 9-10 | 5 | MAX24188 JTAG header. When not in JTAG mode the JTRST pin should be driven low by connecting pins 9 and 10. |
| JB1 | 2x5 header (just below the company logo) | Not jumpered | 8 | Connects to several GPIO on the processor to provide for future board application options. |

## 7. Component List

| DESIGNATION | QTY | DESCRIPTION | SUPPLIER | PART |
|---|---|---|---|---|
| Reference designators shown on next row (C1, …, CB143) | 81 | 0402 CERAM 1uF 10V | TDK | C1005X5R1A105M |
| C1, C2, C12, C13, C14, C22, C27, CB8, CB10, CB13, CB14, CB21, CB23, CB25, CB28, CB30, CB31, CB34, CB35, CB36, CB37, CB38, CB39, CB40, CB41, CB42, CB45, CB49, CB50, CB51, CB52, CB53, CB54, CB55, CB57, CB58, CB62, CB64, CB66, CB67, CB69, CB70, CB71, CB73, CB74, CB76, CB77, CB79, CB81, CB84, CB86, CB87, CB89, CB91, CB92, CB94, CB95, CB98, CB99, CB100, CB102, CB104, CB106, CB107, CB113, CB115, CB116, CB119, CB121, CB122, CB123, CB124, CB127, CB128, CB129, CB133, CB134, CB135, CB141, CB142, CB143 | | | | |
| Reference designators shown on next row (C3, …, CB145) | 41 | 0402 CERAM 0.01uF 16V 10% | Panasonic | ECJ-0EB1C103K |
| C3, C8, C10, C17, C24, CB3, CB7, CB12, CB26, CB27, CB47, CB59, CB60, CB61, CB63, CB65, CB68, CB72, CB75, CB78, CB80, CB82, CB83, CB85, CB88, CB90, CB93, CB96, CB97, CB101, CB103, CB105, CB108, CB109, CB110, CB111, CB114, CB117, CB118, CB120, CB145 | | | | |
| C4, C9, C11, C15, C16, C18, C19, C20, C21, C23, C25, C26, CB1, CB2, CB4, CB5, CB9, CB11, CB15, CB19, CB20, CB24, CB29, CB32, CB33, CB44, CB46, CB56, CB112, CB125, CB130, CB131, CB132, CB139, CB140, CB146 | 36 | 0603 CERAM 10uF 6.3V 20% MULTILAYER | Panasonic | ECJ-1VB0J106M |
| C5, CB18 | 2 | 0603 CERAM .1uF 16V 20% X7R | AVX | 0603YC104MAT |
| C6, C7 | 2 | 0603 CERAM 22pF 25V 5% NPO | AVX | 06033A220JAT |
| CB17, CB22 | 2 | 0603 CERAM 4.7uF 6.3V MULTILAYER | UNK | ECJ-1VB0J475M |
| CB43, CB48, CB126, CB136, CB137, CB138 | 6 | CAP CER 3.3UF 4.0V X5R 0402 | AMK | AMK105BJ335MV-F |
| CB6, CB16, CB144 | 3 | D CASE TANT 470uF 6.3V 20% | KEM | T491D477M006AS |
| DB1 | 1 | SCHOTTKY DIODE, 1 AMP 40 VOLT | International Rectifier | 10BQ040 |
| DS1, DS2, DS3, | 11 | LED, GREEN, SMD | Panasonic | LN1351C |
| DS4, DS15, DS16 | 3 | LED, GREEN, SMD | Panasonic | LN1351C |
| DS9, DS10 | 2 | LED, RED, SMD | Panasonic | LN1251C |
| GND_TP1, GND_TP2, GND_TP3, GND_TP4 | 4 | STANDARD GROUND CLIP | KEYSTONE | 4954 |
| J1 | 1 | 2.0MM SURFACE MOUNT POWER JACK | CUI INC | PJ-002AH-SMT |
| J11 | 1 | 2 PIN HEADER, .100 CENTERS, VERTICAL | Samtec | TSW-102-07-T-S |
| J13, J34 | 4 | TERMINAL STRIP, 10 PIN, DUAL ROW, VERT | DIG | S2012-05-ND |
| J15 | 1 | HEADER, 14 PIN, DUAL ROW, VERT NOT POPULATED | Samtec | HDR-TSW-107-14-T-D |
| J2 | 1 | TYPE B SINGLE RT ANGLE, BLACK | MOL | NA |
| J3, J10, J16, J17, J18 | 6 | CONNECTOR, SMB, 50 OHM VERTICAL, 5PIN | AMP | 413990-1 |
| J4, J8, J22, J23, J24, J25, J26, J27, J28 | 11 | 100 MIL 2 POS JUMPER | NA | NA |
| J5, J6, J9, J14, J19 | 5 | TERMINAL STRIP, 6 PIN, DUAL ROW, VERT | Samtec | TSW-103-07-T-D |
| JB1 J15, J21 | 3 | TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPULATE | DNP | DNP |
| JP1, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP23, JP24, JP25, JP26, JP27, JP28, JP29, JP30 | 34 | 100 MIL 3 POS JUMPER | NA | NA |
| LB1, LB3, LB4, LB9, LB10, LB11, LB12, LB13, LB14 | 9 | FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD | Steward | HI1206N101R-00 |

| DESIGNATION | QTY | DESCRIPTION | SUPPLIER | PART |
|---|---|---|---|---|
| LB5, LB6, LB7, LB8 | 4 | 1uH ±10% 0805 Multilayer Ceramic 400 mA (ok to sub with 445-3156-1-ND) | Murata | LQM21FN1R0N00D |
| R1, R4, R5, R6, R7, R9, R10, RB5 | 9 | RES 0603 30 Ohm 1/16W | Panasonic | ERJ-3GEYJ300V |
| R11, R18, R19, R21, R57, RB8, RB3 | 4 | RES 0402 0 OHM 1/10W 5% | Panasonic | ERJ-2GE0R00X |
| R12, R17, R20, R22, R23, R29, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56 | 32 | RES 0201 30.0 OHM 1/16W 1% | Panasonic | ERJ-1GEJ300C |
| R13, R14, R25, R26, RB23, RB24, RB25, RB38, RB44, RB45, RB49, RB50, RB51, RB52, RB53, RB54, RB56, RB57, RB63, RB64, RB69, RB71, RB72, RB73, RB77, RB78, RB79, RB80, RB81, RB86, RB87, | 31 | RES 0402 10.0 KOHM 1/16W 1% | Panasonic | ERJ-2RKF1002X |
| R16, RB27, RB28, RB29 | 4 | RES 0402 30.0 OHM 1/16W 1% | Panasonic | ERJ-2RKF30R0X |
| R30, R15 | 2 | RES 0402 100 OHM 1/16W 1% | Panasonic | ERJ-2RKF1000X |
| R2, R3 | 2 | RES 0603 33.2 Ohm 1/16W 1% | Panasonic | ERJ-3EKF33R2V |
| R24, R28, R62, R63, RB13, RB15, RB16, RB17, RB18, RB19, RB20, RB21, RB22, RB26, RB39, RB40, RB41, RB42, RB43, RB82 | 18 | RES 0402 1.00 KOHM 1/16W 1% | Panasonic | ERJ-2RKF1001X |
| R27 | 1 | RES 0402 1.40 KOHM 1/16W 1% | Panasonic | ERJ-2RKF1401X |
| R8 | 1 | RES 0603 1.00M Ohm 1/16W 1% | Panasonic | ERJ-3EKF1004V |
| RB1, RB4, RB9, RB30, RB31, RB32, RB33, RB34, RB60, RN1 | 11 | RES 0603 1.0K Ohm 1/16W 5% | Panasonic | ERJ-3GEYJ102V |
| RB14, RB84, RB85, R60 | 5 | RES 0603 330 Ohm 1/16W 5% | Panasonic | ERJ-3GEYJ331V |
| RB2, RB11, RB35, RB36, RB37 | 5 | RES 0402 49.9 OHM 1/16W 1% | Panasonic | ERJ-2RKF49R9X |
| RB6, RB10, RB83 | 3 | RES 0603 10K Ohm 1/16W 5% | Panasonic | ERJ-3GEYJ103V |
| RB65 | 1 | RES 0603 2.49K Ohm 1/16W 1% | Panasonic | ERJ-3EKF2491V |
| RB7 | 1 | RES 0603 10.0K Ohm 1/16W 1% | Panasonic | ERJ-3EKF1002V |
| RPB5, RPB6, RPB7, RPB9, RPB13 | 6 | RESISTOR, 4 PACK, 330 OHM 5PCT QUAD 0603 | Panasonic | EXB-V8V331JX |
| RPB10, RPB11 | 2 | RESISTOR, 4 PACK, 10K OHM 5PCT QUAD 0603 | Panasonic | EXB-V8V103JX |
| RPB2, RPB3, RPB4 | 3 | RESISTOR, 4 PACK, 33 OHM 5PCT QUAD 0603 | Panasonic | EXB-V8V330JV |
| RPB8, RPB12 | 2 | RESISTOR, 4 PACK, 4.7K OHM 5PCT QUAD 0603 | Panasonic | EXB-V8V472JX |
| SW1 | 1 | SWITCH MOM 4PIN SINGLE POLE | Panasonic | EVQPAE04M |
| TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP15,TP16,TP17,TPB1,TPB2,TPB3,TPB4,TPB5,TPB6,TPB7,TPB8,TPB9,TPB10 | 26 | TESTPOINT, 1 PLATED HOLE, DO NOT STUFF | NA | NA |
| U1 | 1 | MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143 | Maxim | MAX811TEUS-T |
| U2 | 1 | VOLTAGE MONITOR 5, 3.3, 2.5, ADJ | Maxim | MAX6709AUB+ |
| UB3,UB4,UB5,UB6,UB9,UB10,UB11,UB12,UB13,UB14,UB15,UB16,UB19,UB20 | 14 | HIGH SPEED BUFFER | FAIRCHILD | NC7SZ86 |
| U4 | 1 | IC, HCS08 8-BIT MICROCONTROLLER, 32K FLASH, 2K RAM, 2 UART, 2 SPI, I2C, USB, -40 TO 85C, 64 PIN LQFP | FREESCALE | MC9S08JM32CLH-ND |
| U5 | 1 | RTL8363 PHY | REALTEK | RTL8363C |
| U6 | 1 | MAX24188 QFN 8X8 | MICROSEMI | MAX24188ETK+ |
| U7 | 1 | SFP host / receptacle | PARTS_KIT | SFP_HOST-TYCO |

| DESIGNATION | QTY | DESCRIPTION | SUPPLIER | PART |
|---|---|---|---|---|
| U8 | 1 | IC, LINEAR REG ADJ, 2A, 14TSSOP-EP | MAXIM | MAX8526EUD+ |
| UB2, UB7, UB17, UB18, UB21 | 5 | IC, LINEAR REGULATOR, 1.5W, 3.3V OR ADJ, 1A, 16 PIN TSSOP-EP | Maxim | MAX1793EUE-33 |
| XB1 | 1 | XTAL, HC49SD, 12.0000MHz +/-50PPM, CL=20PF | FOX | FOXSDLF-120-20 |
| Y1 | 1 | OSCILLATOR LVCMOS, 3.3V, 25 MHZ, 4 PIN SMD | Connor-Winfield | MX010-025.0M |
| Y2 | 1 | OSCILLATOR, VECTRON OCXO, 3.3V, 12.8 MHZ, 5 PIN THROUGH-HOLE | VEC | MC853X4-035W |
| Y3 | 1 | OSCILLATOR, RAKON TC-OCXO, 3.3V, 10MHZ RFPO-30-RX-C-LF | RAKON | P5299LF |
| J9 | 1 | TERMINAL STRIP, 6 PIN, DUAL ROW, VERT NOT POPULATED | Samtec | TSW-103-07-T-D NOT POPULATED |
| TP14 | 1 | TESTPOINT, 1 PLATED HOLE RED | KEYSTONE | 5000R |
| U3,UB1,UB8 | 3 | TINYLOGIC HIGH SPEED 2-INPUT AND GATE, 5 PIN SOT23 | Fairchild | NC7SZ08M5 |

**Not Populated:**
DS5, DS6, DS7, DS8, DS9, DS10, DS11, DS12, DS13, DS14
J7, J12, J29, J30, J31, J32, J33, JP2, JP20, JP21, JP22, JP31, JP32, JP33, JP34
U5, U7

## 8. Schematics

The MAX24188 EV Kit board design is a bill of materials modification of the MAX24287 EV Kit. See the following pages for the MAX24287 EV Kit schematics. The list of components that are not populated in the MAX24188 EV Kit board is shown at the end of section 7 above.

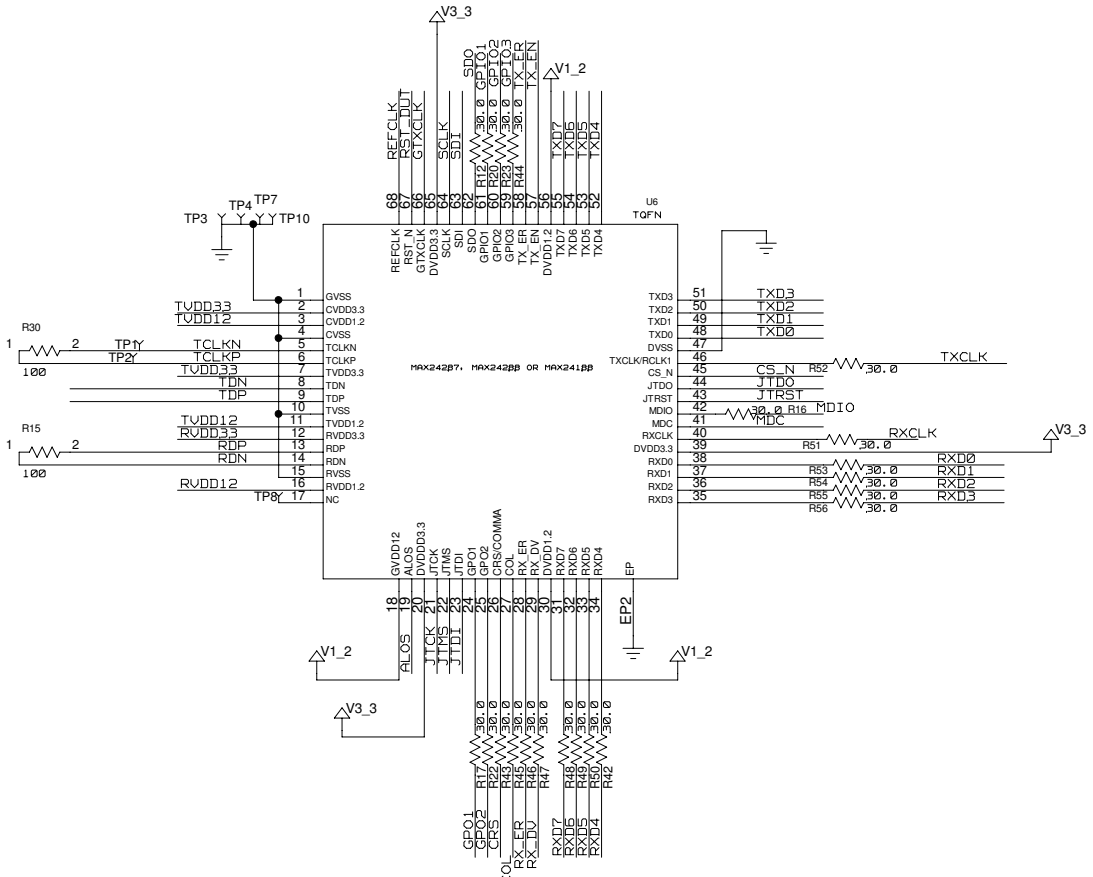
## 9. Ordering Information

| PART | TYPE |
|---|---|
| MAX24188EVKIT | Evaluation Kit |

## 10. Revision History

| REVISION DATE | DESCRIPTION |
|---|---|
| 10/11 | Initial Release |
| 2012-05 | Reformatted for Microsemi. No content change. |

# MAX24287 EVKIT Rev_B

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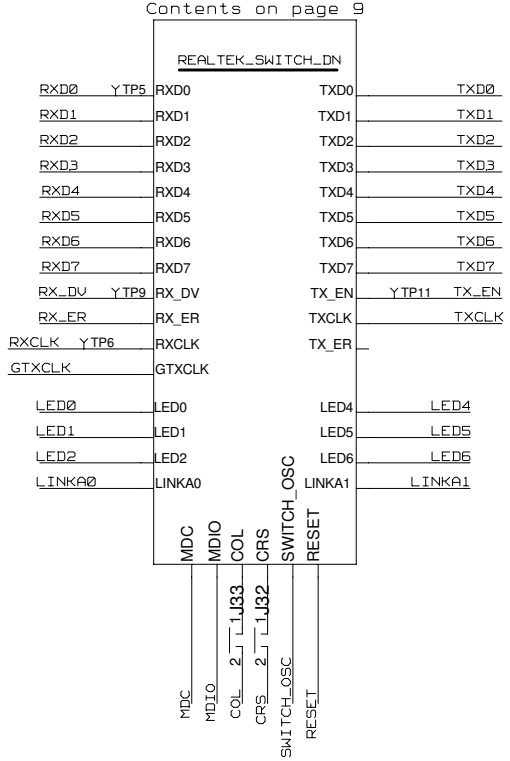
| ENGINEER: Steve Scully | PAGE: 1/11 (TOTAL) 1/B (BLOCK) |

Switch Hierarchy block.
Contents on page 9

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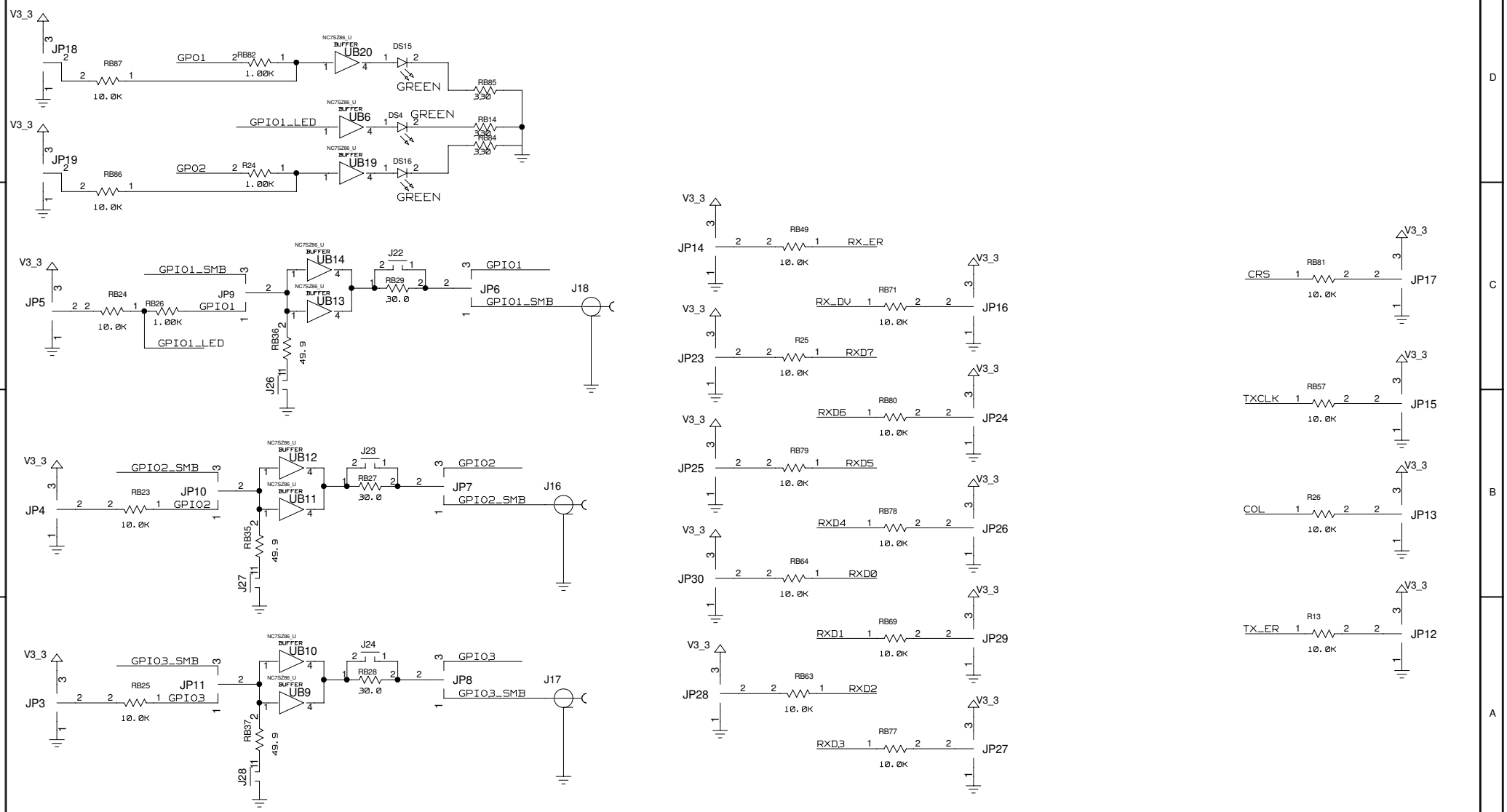


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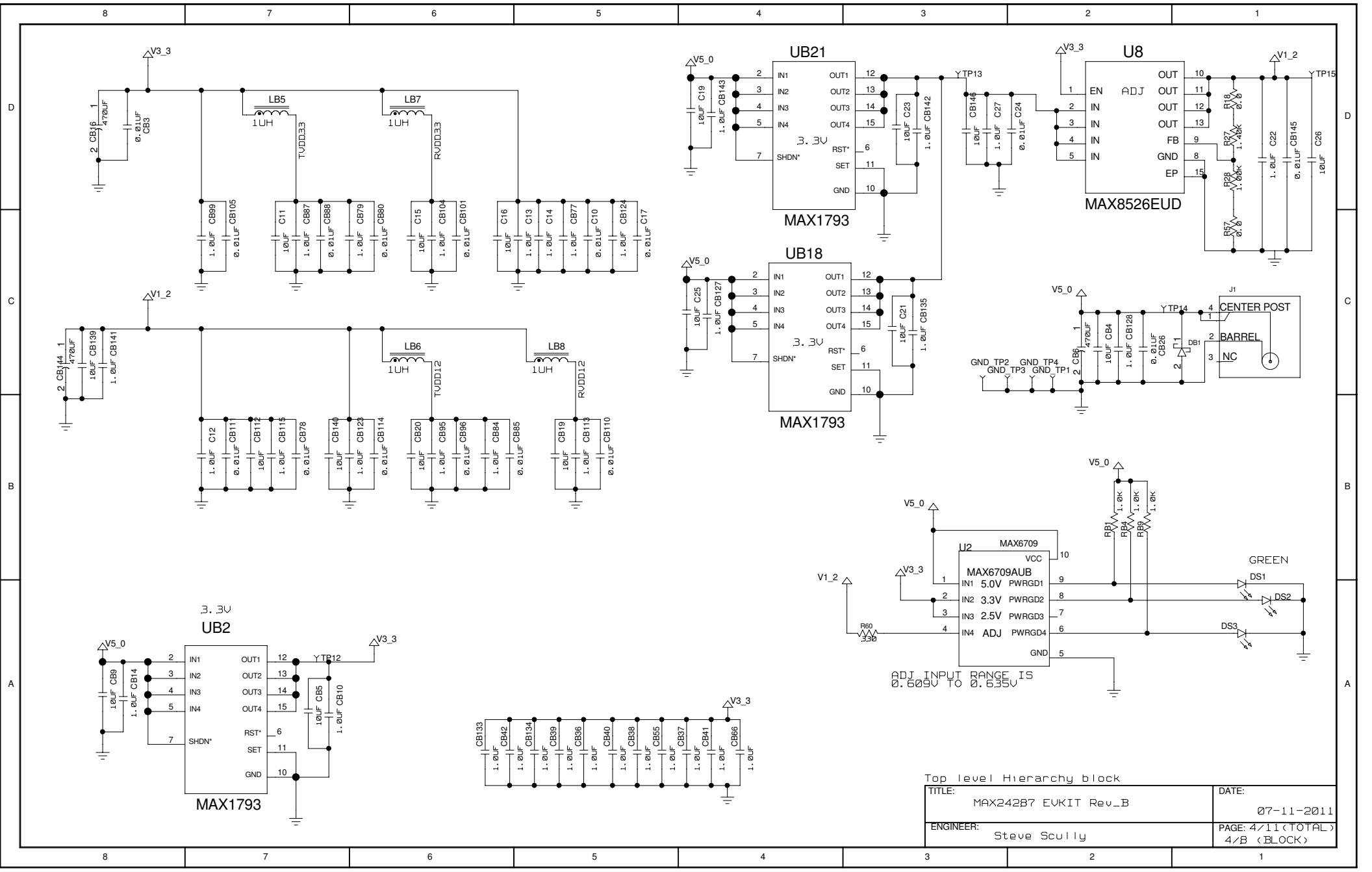
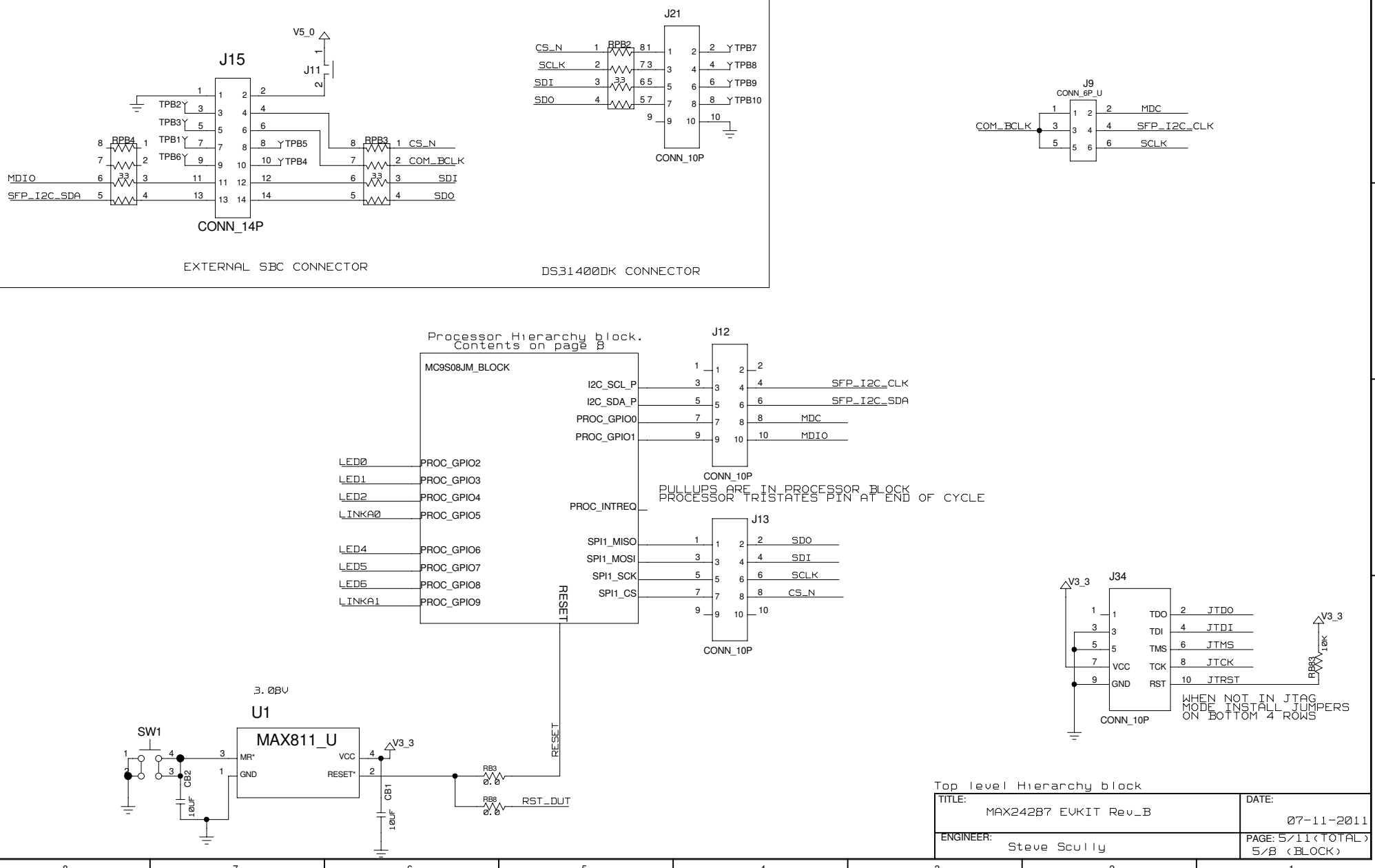

UB21
MAX1793
UB18
MAX1793
U8
MAX8526EUD
UB2
MAX1793
U2
MAX6709
MAX6709AUB
ADJ INPUT RANGE IS
0.609V TO 0.635V
GREEN
CENTER POST
BARREL
NC
Top level Hierarchy block
TITLE:
MAX24287 EVKIT Rev_B
DATE:
07-11-2011
ENGINEER:
Steve Scully
PAGE: 4/11 (TOTAL)
4/8 (BLOCK)

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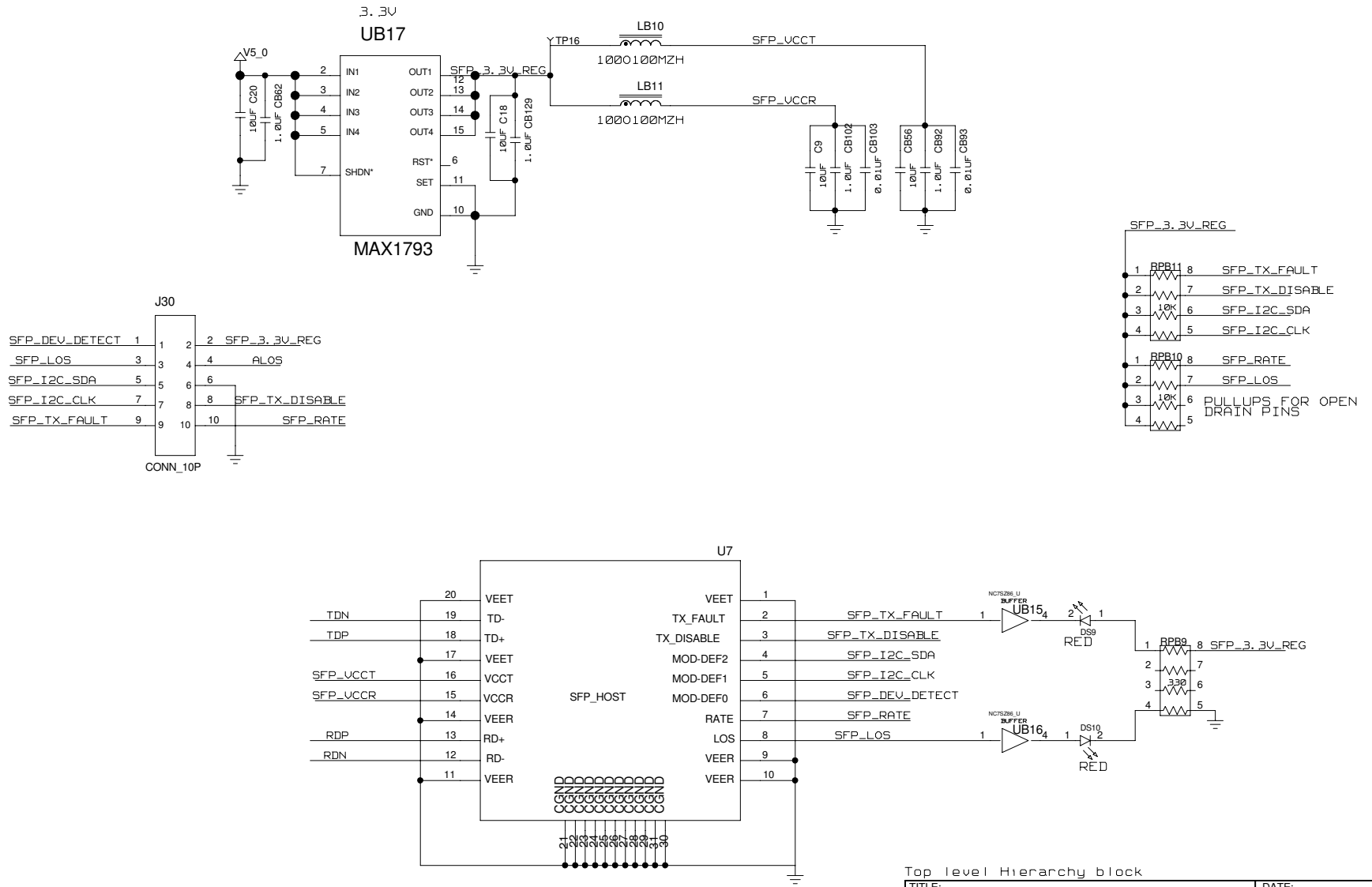


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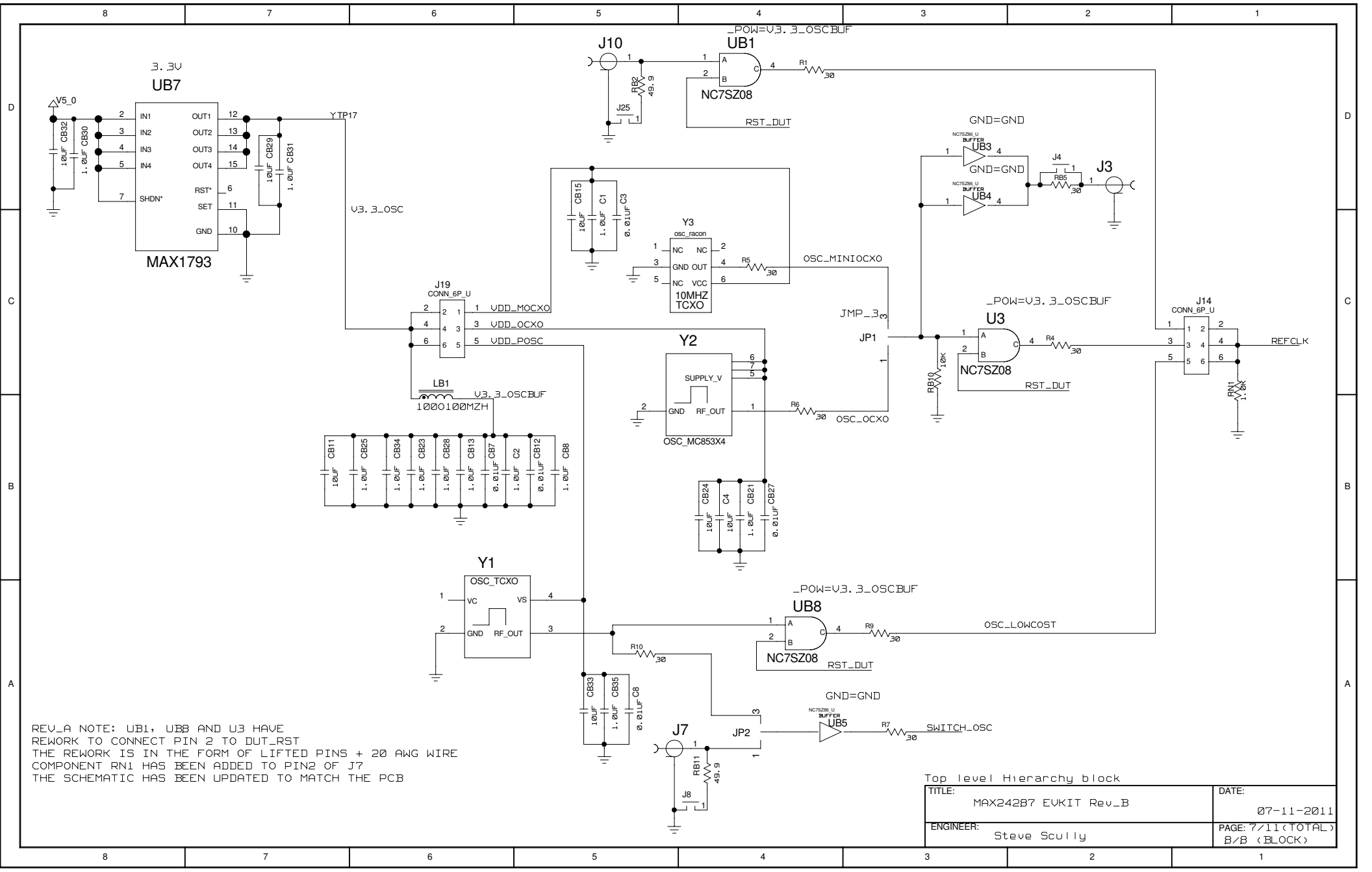
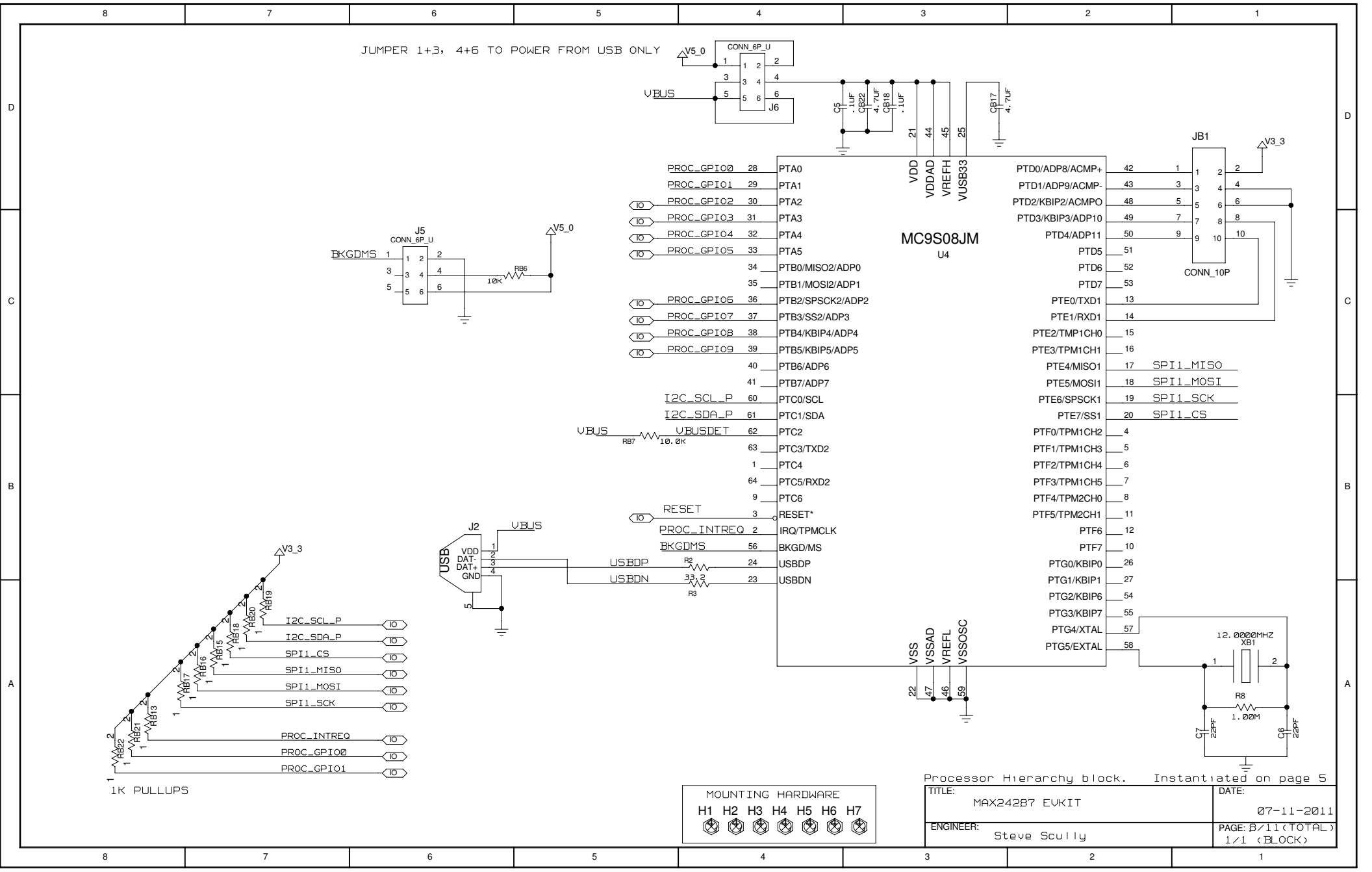
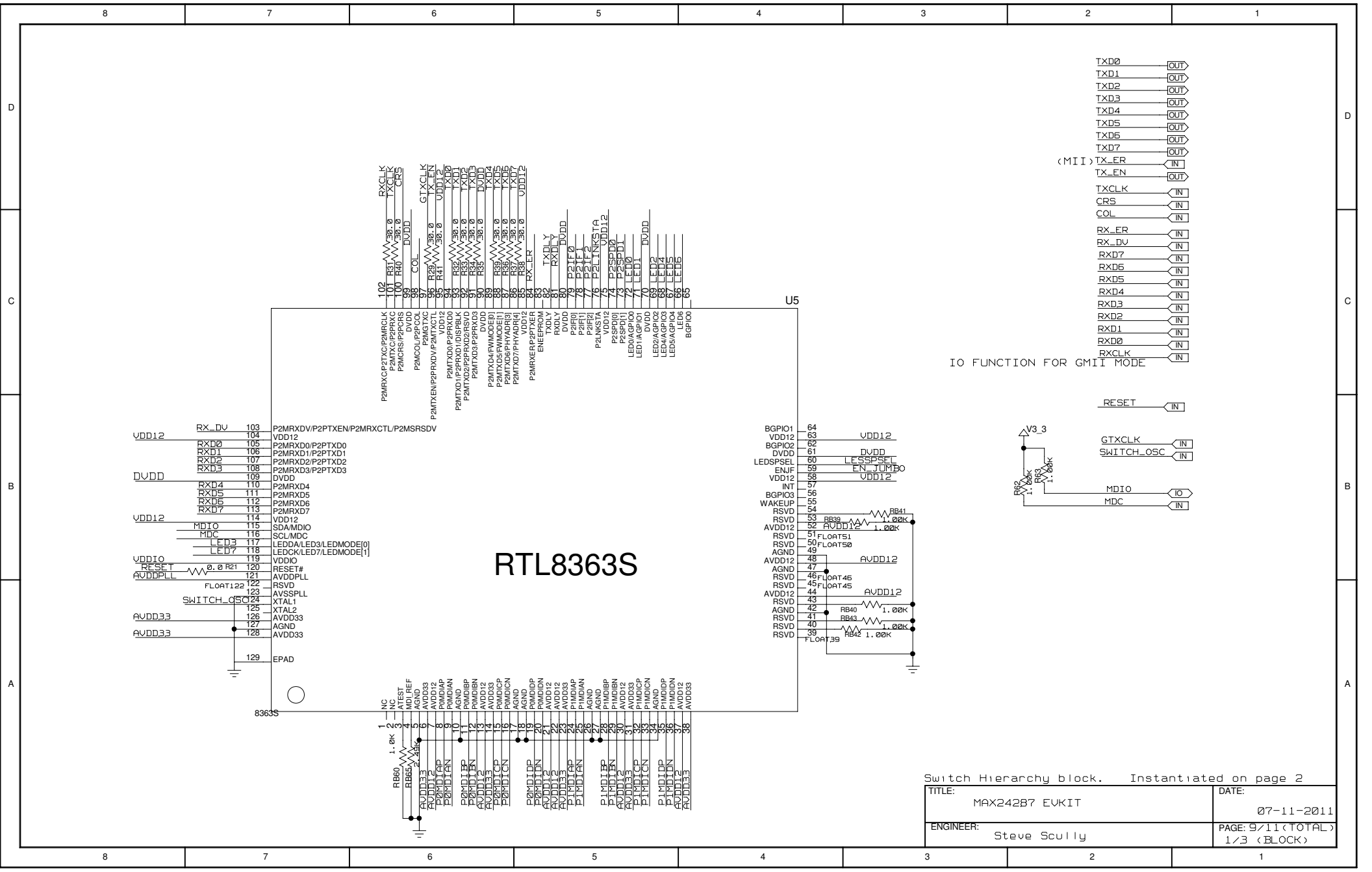


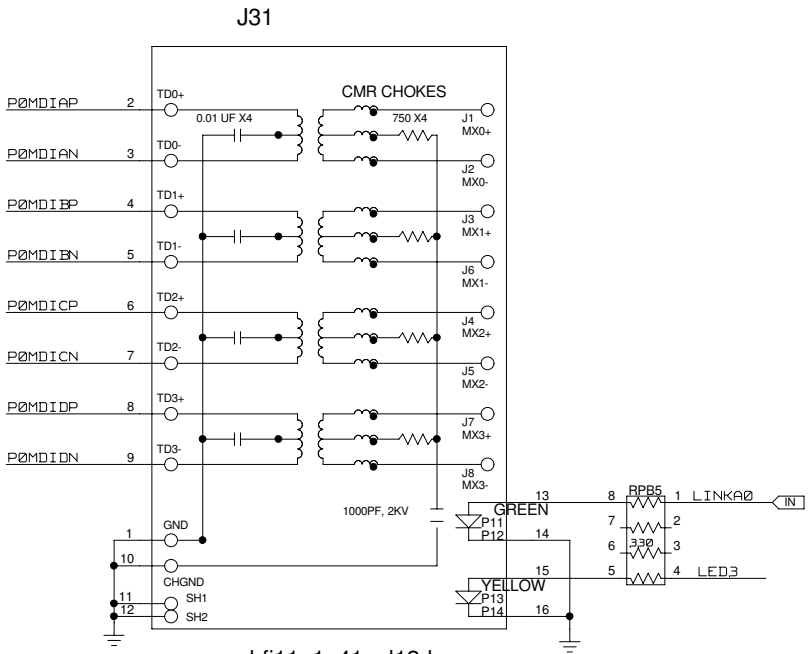

REV_A NOTE: UB1, UB8 AND U3 HAVE
REWORK TO CONNECT PIN 2 TO DUT_RST
THE REWORK IS IN THE FORM OF LIFTED PINS + 20 AWG WIRE
COMPONENT RN1 HAS BEEN ADDED TO PIN2 OF J7
THE SCHEMATIC HAS BEEN UPDATED TO MATCH THE PCB

Top level Hierarchy block

| | |
|---|---|
| TITLE: MAX24287 EVKIT Rev_B | DATE: 07-11-2011 |
| ENGINEER: Steve Scully | PAGE: 7/11(TOTAL) 8/8 (BLOCK) |


JUMPER 1+3, 4+6 TO POWER FROM USB ONLY
V5_0
CONN_6P_U
VBUS
J6
C5 .1UF
CB22 4.7UF
CB18 .1UF
CB17 4.7UF
VDD
VDDAD
VREFH
VUSB33
MC9S08JM
U4
PTA0
PTA1
PTA2
PTA3
PTA4
PTA5
PTB0/MISO2/ADP0
PTB1/MOSI2/ADP1
PTB2/SPSCK2/ADP2
PTB3/SS2/ADP3
PTB4/KBIP4/ADP4
PTB5/KBIP5/ADP5
PTB6/ADP6
PTB7/ADP7
PTC0/SCL
PTC1/SDA
PTC2
PTC3/TXD2
PTC4
PTC5/RXD2
PTC6
RESET*
IRQ/TPMCLK
BKGD/MS
USBDP
USBDN
PROC_GPIO0
PROC_GPIO1
PROC_GPIO2
PROC_GPIO3
PROC_GPIO4
PROC_GPIO5
PROC_GPIO6
PROC_GPIO7
PROC_GPIO8
PROC_GPIO9
I2C_SCL_P
I2C_SDA_P
VBUSDET
RESET
PROC_INTREQ
BKGDMS
J5
CONN_6P_U
BKGDMS
RB6
10K
RB7
10.0K
J2
USB
VDD
DAT-
DAT+
GND
R2
33.2
R3
JB1
CONN_10P
V3_3
PTD0/ADP8/ACMP+
PTD1/ADP9/ACMP-
PTD2/KBIP2/ACMPO
PTD3/KBIP3/ADP10
PTD4/ADP11
PTD5
PTD6
PTD7
PTE0/TXD1
PTE1/RXD1
PTE2/TMP1CH0
PTE3/TPM1CH1
PTE4/MISO1
PTE5/MOSI1
PTE6/SPSCK1
PTE7/SS1
SPI1_MISO
SPI1_MOSI
SPI1_SCK
SPI1_CS
PTF0/TPM1CH2
PTF1/TPM1CH3
PTF2/TPM1CH4
PTF3/TPM1CH5
PTF4/TPM2CH0
PTF5/TPM2CH1
PTF6
PTF7
PTG0/KBIP0
PTG1/KBIP1
PTG2/KBIP6
PTG3/KBIP7
PTG4/XTAL
PTG5/EXTAL
VSS
VSSAD
VREFL
VSSOSC
12.0000MHZ
XB1
R8
1.00M
C7 22PF
C6 22PF
RB19
RB20
RB18
RB15
RB16
RB17
RB13
RB21
RB22
1K PULLUPS
MOUNTING HARDWARE
H1 H2 H3 H4 H5 H6 H7
Processor Hierarchy block. Instantiated on page 5
TITLE: MAX24287 EVKIT
DATE: 07-11-2011
ENGINEER: Steve Scully
PAGE: 8/11 (TOTAL)
1/1 (BLOCK)


RTL8363S
U5
8363S
IO FUNCTION FOR GMII MODE
(MII)
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
TX_ER
TX_EN
TXCLK
CRS
COL
RX_ER
RX_DV
RXD7
RXD6
RXD5
RXD4
RXD3
RXD2
RXD1
RXD0
RXCLK
RESET
V3_3
GTXCLK
SWITCH_OSC
MDIO
MDC
Switch Hierarchy block. Instantiated on page 2
TITLE: MAX24287 EVKIT
DATE: 07-11-2011
ENGINEER: Steve Scully
PAGE: 9/11 (TOTAL) 1/3 (BLOCK)

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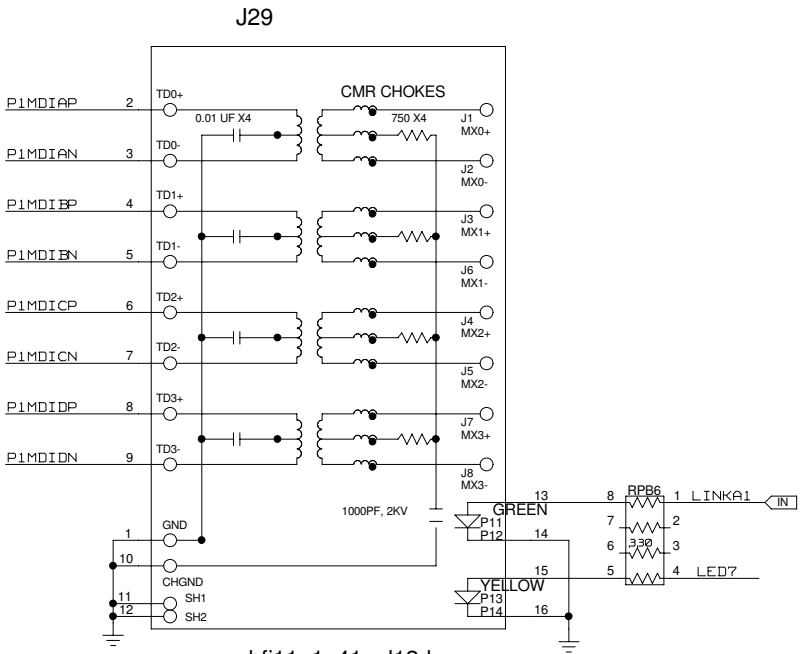



conn_hfj11_1g41e_l12rl

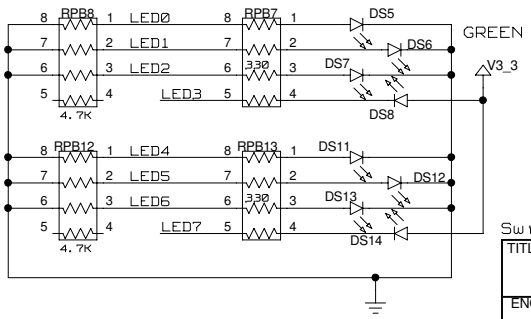
INDICATIONS FOR PARALLEL MODE0

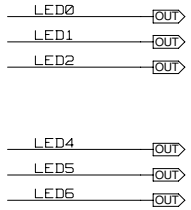
SWITCH0

LED0=GIG_LINK/ACT
LED1=100_LINK/ACT
LED2=10_LINK/ACT
LED3=DUP/COL

SWITCH1

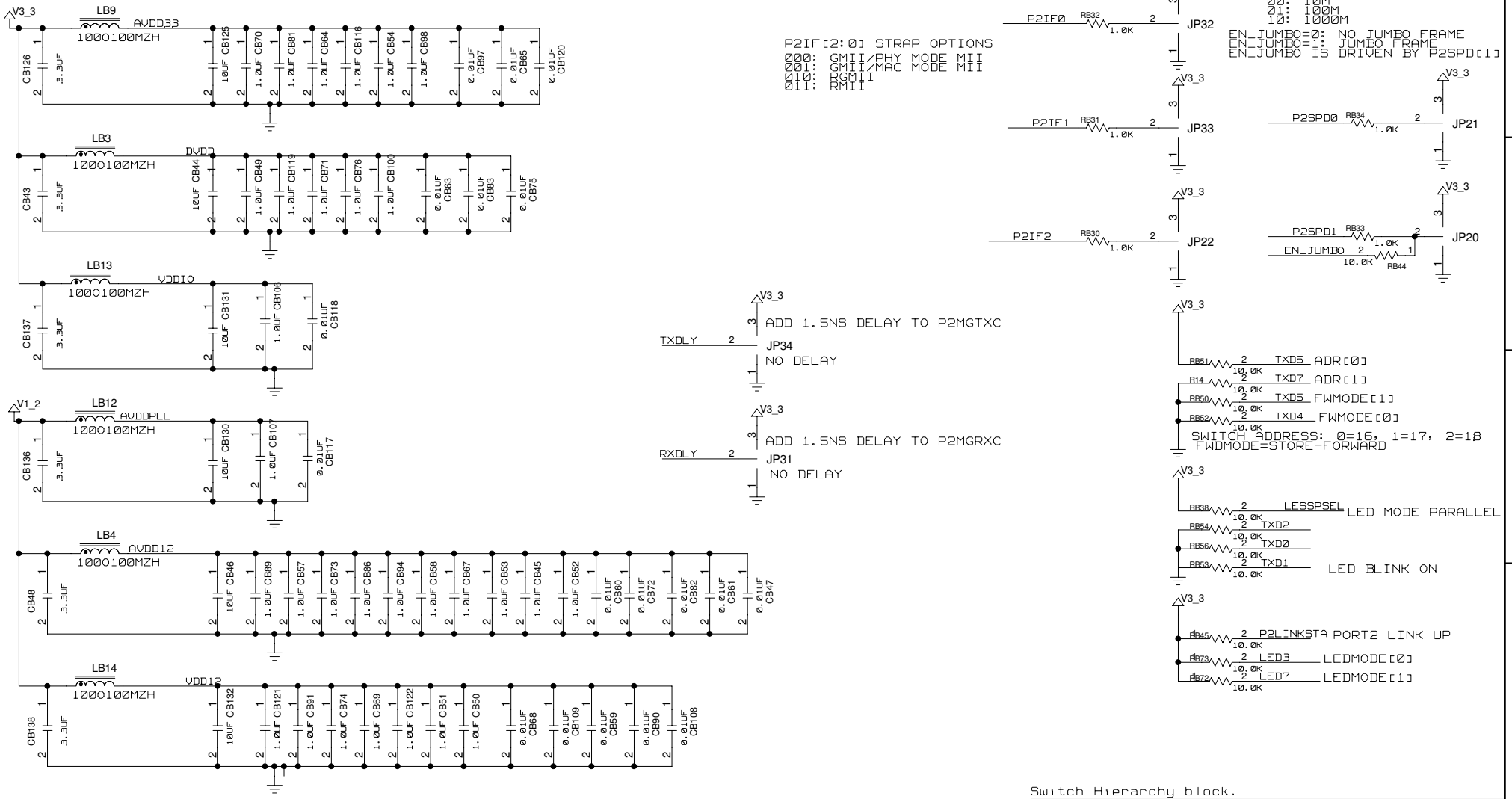
LED4=GIG_LINK/ACT
LED5=100_LINK/ACT
LED6=10_LINK/ACT
LED7=DUP/COL




Switch Hierarchy block.

| | |
|---|---|
| TITLE: MAX24287 EVKIT | DATE: 07-11-2011 |
| ENGINEER: Steve Scully | PAGE: 10/11 (TOTAL) 2/3 (BLOCK) |




Switch Hierarchy block.

| | |
|---|---|
| TITLE: MAX24287 EVKIT | DATE: 07-11-2011 |
| ENGINEER: Steve Scully | PAGE: 11/11 (TOTAL) 3/3 (BLOCK) |

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Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.